AMENDMENTS TO THE CLAIMS

1. (Previously presented) A semiconductor device comprising:

a first semiconductor chip consisting of at least either a circuit against static damage or a passive component;

a second semiconductor chip and a third semiconductor chip installed on a support substrate, wherein said second semiconductor chip and said third semiconductor chip are connected with each other through said first semiconductor chip; and

wherein said second semiconductor chip is a DRAM chip, and said third semiconductor chip is a logic chip.

2. (Original) The semiconductor device according to claim 1, wherein said passive component includes at least one of a resistor, a capacitor and a reactor.

3. (Original) The semiconductor device according to claim 1, wherein said first semiconductor chip consists of only said passive component.

4-5. (Cancelled)

6. (Previously presented) The semiconductor device according to claim 1, wherein

said second semiconductor chip and said third semiconductor chip include no circuits against static damage.

7-8. (Cancelled)

9. (Previously presented) A semiconductor device comprising:

a plurality of semiconductor chips installed on a support substrate;

a wire connecting said plurality of semiconductor chips with each other and having a passive component function; and

wherein said wire having a passive component function has a length greater than that for linearly connecting terminals of said plurality of semiconductor chips with each other thereby forming a resistive element.

10. (Previously presented) A semiconductor device comprising:

a plurality of semiconductor chips installed on a support substrate;

a wire connecting said plurality of semiconductor chips with each other and having a passive component function; and

a dummy wire fixed to a prescribed potential and arranged to be opposed to said wire at a prescribed interval, wherein said wire is combined with said dummy wire to form a capacitor.

11. (Previously presented) The semiconductor device according to claim 9, wherein

said wire is formed either in a single layer or in two layers.

12. (Original) A semiconductor device having a plurality of semiconductor chips installed on a support substrate, wherein

at least one of said semiconductor chips includes:

a first input/output terminal, employed for testing an independent operating state of said semiconductor chip, having a first circuit against static damage,

a second input/output terminal, employed for connecting said semiconductor chip to said support substrate, having a second circuit against static damage, and

a third input/output terminal other than said first input/output terminal and said second input/output terminal, and

said plurality of semiconductor chips are connected with each other through said third input/output terminal.

13. (Original) The semiconductor device according to claim 12, wherein said third input/output terminal includes no circuit against static damage.

14. (Original) The semiconductor device according to claim 13, wherein said third input/output terminal includes only a resistor.

15. (Original) The semiconductor device according to claim 12, wherein said third input/output terminal includes a third circuit against static damage, and

a transistor forming said third circuit against static damage is smaller than transistors forming said first and second circuits against static damage.

16. (Original) The semiconductor device according to claim 15, wherein

the gate width of said transistor forming said third circuit against static damage is smaller than the gate width of said transistors forming said first and second circuits against static damage.

17. (Original) The semiconductor device according to claim 12, wherein said third input/output terminal includes a third circuit against static damage, said third circuit against static damage is formed by a diode, and said first and second circuits against static damage are formed by transistors.

18. (Original) The semiconductor device according to claim 12, wherein said plurality of semiconductor chips include a DRAM chip and a logic chip.

19. (Original) A semiconductor device having a plurality of semiconductor chips installed on a support substrate, wherein

at least one of said semiconductor chips includes:

a first input/output terminal and a second input/output terminal,

a first circuit against static damage connected to said first input/output terminal, and

switching means connected between said first input/output terminal and said first circuit against static damage and on-off controlled by said second input/output terminal.

20. (Original) The semiconductor device according to claim 19, wherein said switching means is set to an ON state by applying no voltage to said second input/output terminal during a step of fabricating said semiconductor chips and set to an OFF state by applying a prescribed voltage to said second input/output terminal after completion of a chip connection step following fabrication of said semiconductor chips.

21. (Original) The semiconductor device according to claim 19, wherein said first circuit against static damage includes first and second transistors, and said switching means includes:

a third transistor connected between said first transistor and said first input/output terminal to enter an ON state when no voltage is applied to said second input/output terminal and enter an OFF state when said prescribed voltage is applied to said second input/output terminal, and

a fourth transistor connected between said second transistor and said first input/output terminal to enter an ON state when no voltage is applied to said second input/output terminal and enter an OFF state when said prescribed voltage is applied to said second input/output terminal.

22. (Original) The semiconductor device according to claim 19, wherein

a second circuit against static damage is connected to said second input/output terminal.

23. (New) A semiconductor device comprising:

a first semiconductor chip installed on a support substrate, consisting of only a passive component for controlling timing for signal transmission and having a plurality of input/output terminals,

a second semiconductor chip and a third semiconductor chip installed on said support substrate and having an individual function, respectively, wherein

said second semiconductor chip and said third semiconductor chip are connected with each other through said first semiconductor chip by connecting selected ones of said plurality of input/output terminals of said first semiconductor chip, respectively.

24. (New) A semiconductor device according to claim 23, wherein

said passive component for controlling timing includes a first passive sub-component and a second passive sub-component,

said plurality of input/output terminals of said first semiconductor chip include a first input/output terminal, a second input/output terminal and a third input/output terminal,

said first passive sub-component is connected between said first input/output terminal and said second input/output terminal, and

said second passive sub-component is connected between said first input/output terminal and said third input/output terminal.

25. (New) A semiconductor device according to claim 23, wherein

said passive component for controlling timing includes a first passive sub-component and a second passive sub-component of similar circuit elements,

said plurality of input/output terminal of said first semiconductor chip include a first input/output terminal, a second input/output terminal and a third input/output terminal,

said first passive sub-component is connected between said first input/output terminal and said second input/output terminal, and

said second passive sub-component is connected between said first input/output terminal and said third input/output terminal.

26. (New) A semiconductor device according to claim 23, wherein

said passive component for controlling timing includes a resistor, a capacitor and a reactor.